

MS-7115

Version 1.0

Title	Page
COVER SHEET	1
BLOCK DIAGRAM	2
Intel LGA775	3 , 4 , 5
Intel Grantsdale	6 , 7 , 8 , 9
ICH6	10,11,12
ICS954119 Gen. & FWH	13
LPC I/O - W83627THF&LM86	14
Azalia Audio	15
RTL8110S(B)/8100C	16
DDR DIMM 1 & 2	17
DDR Termination Resistors	18
PCI -Express X16 Port	19
PCI Slot &MINI PCI	20
VIA-6307 IEEE1394 Controller	21
USB CONNECTORS	22
ATX ,Front Panel&LCM&IR	23
MS7 ACPI Controller	24
VRM10.1 Intersil 6565 4Phase	25
SATA1,2 , IDE1& Fan control	26
VGA Connector & Misc	27
EQ&SRS&FRONT AUDIO	28
POWER MAP	29
Clock Distribution Diagram	30
HISTORY	31

PCI Routing Table

PCI Device	IDSEL	REQ/GNT	INTERRUPT
PCI Slot	AD17	1	B
MINI PCI	AD18	2	C
VT6307 IEEE1394	AD19	4	D
RTL8110SB/8100C LAN	AD22	3	C

Intel (R) Grantsdale (GMCH) + ICH6 Chipset
Intel Prescott LGA775 Processor

CPU:

Intel Prescott - 3.0G & Above

System Chipset:

Intel Grantsdale - GMCH (North Bridge)
Intel ICH6 (South Bridge)

On Board Chipset:

BIOS -- FWH EEPROM
AC'97 Codec -- ALC 880
LPC Super I/O -- W83627THF
LAN -- Realtek 8100C/8110SB
EEE1394 -- VIA VT6307
CLOCK -- ICS954119

Main Memory:


DDR 1 * 2 (Max 2GB)

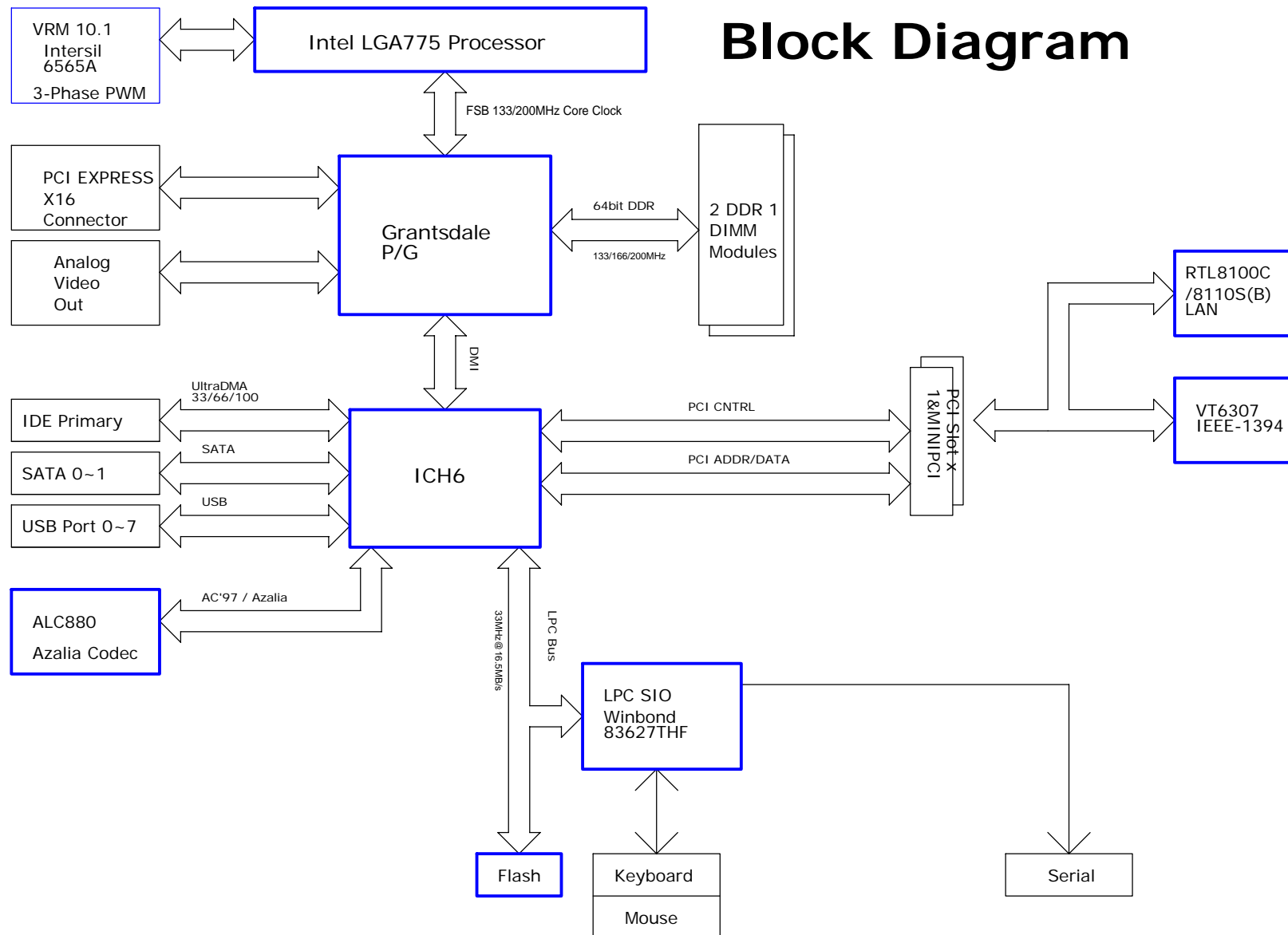
Expansion Slots:

PCI EXPRESS X16 SLOT * 1
PCI 2.3 SLOT * 1
MINI PCI SLOT * 1

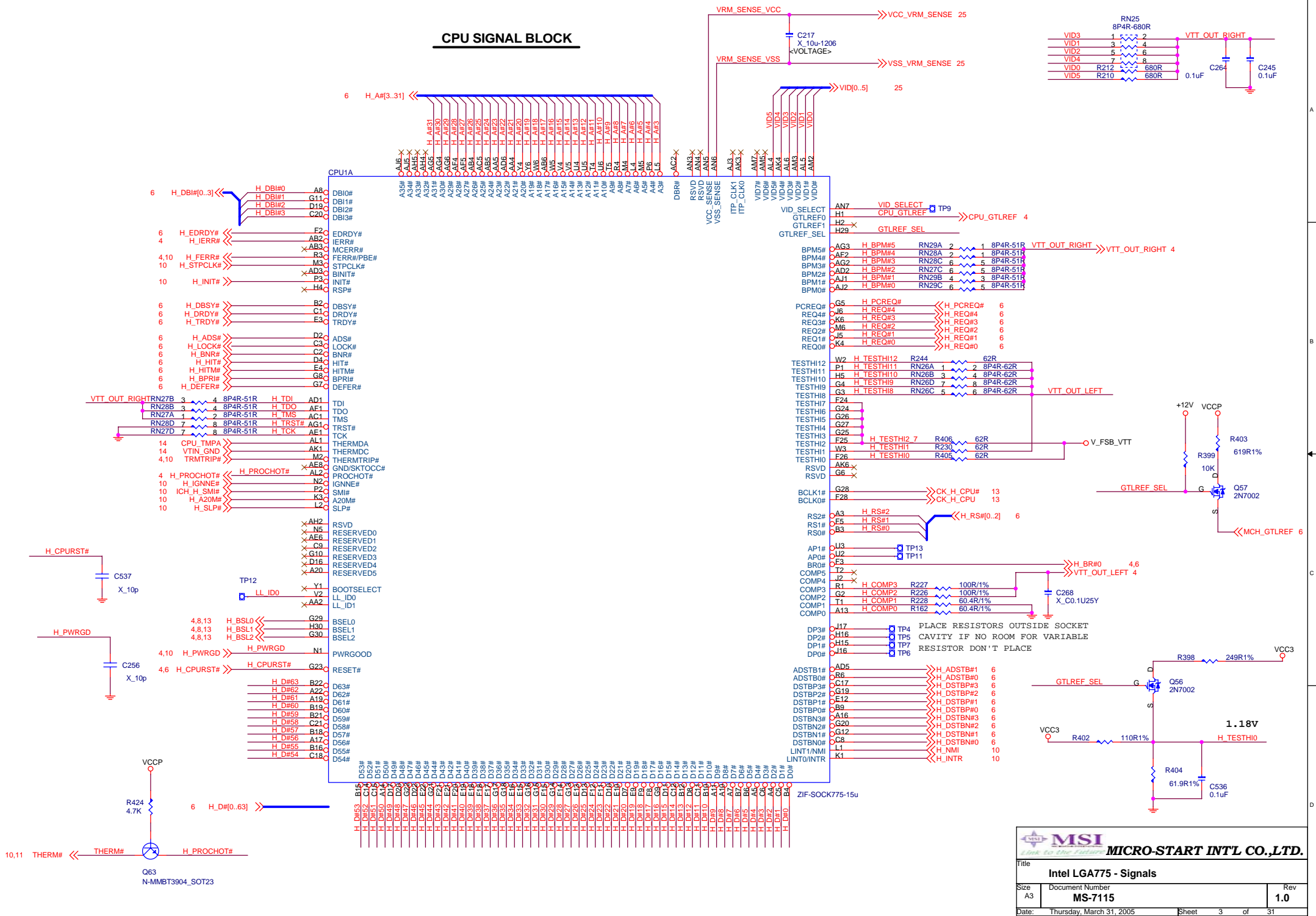
Intersil PWM:

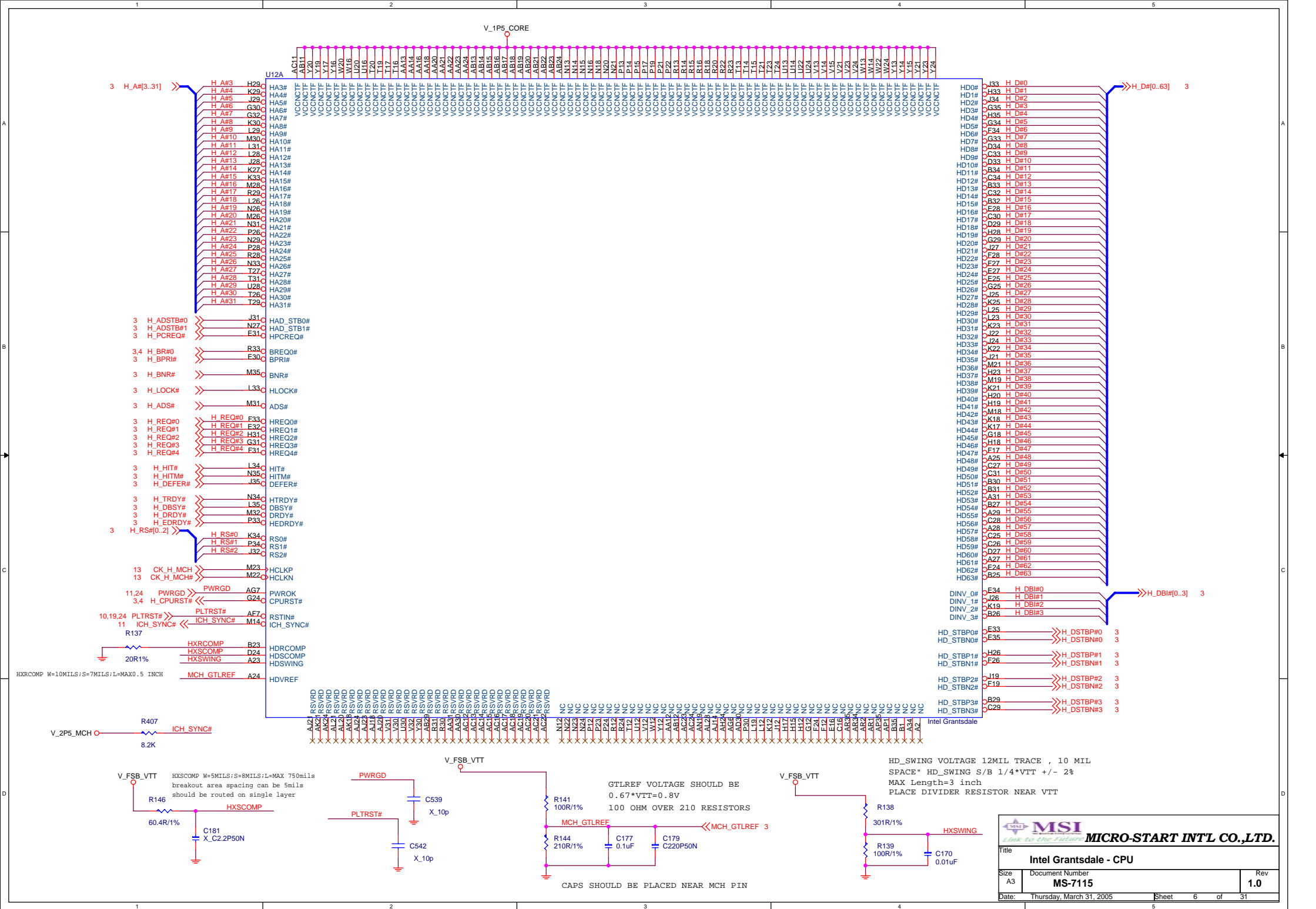
Controller: HIP6561 3 Phase
Driver: HIP6602B * 1 + HIP6601B * 1

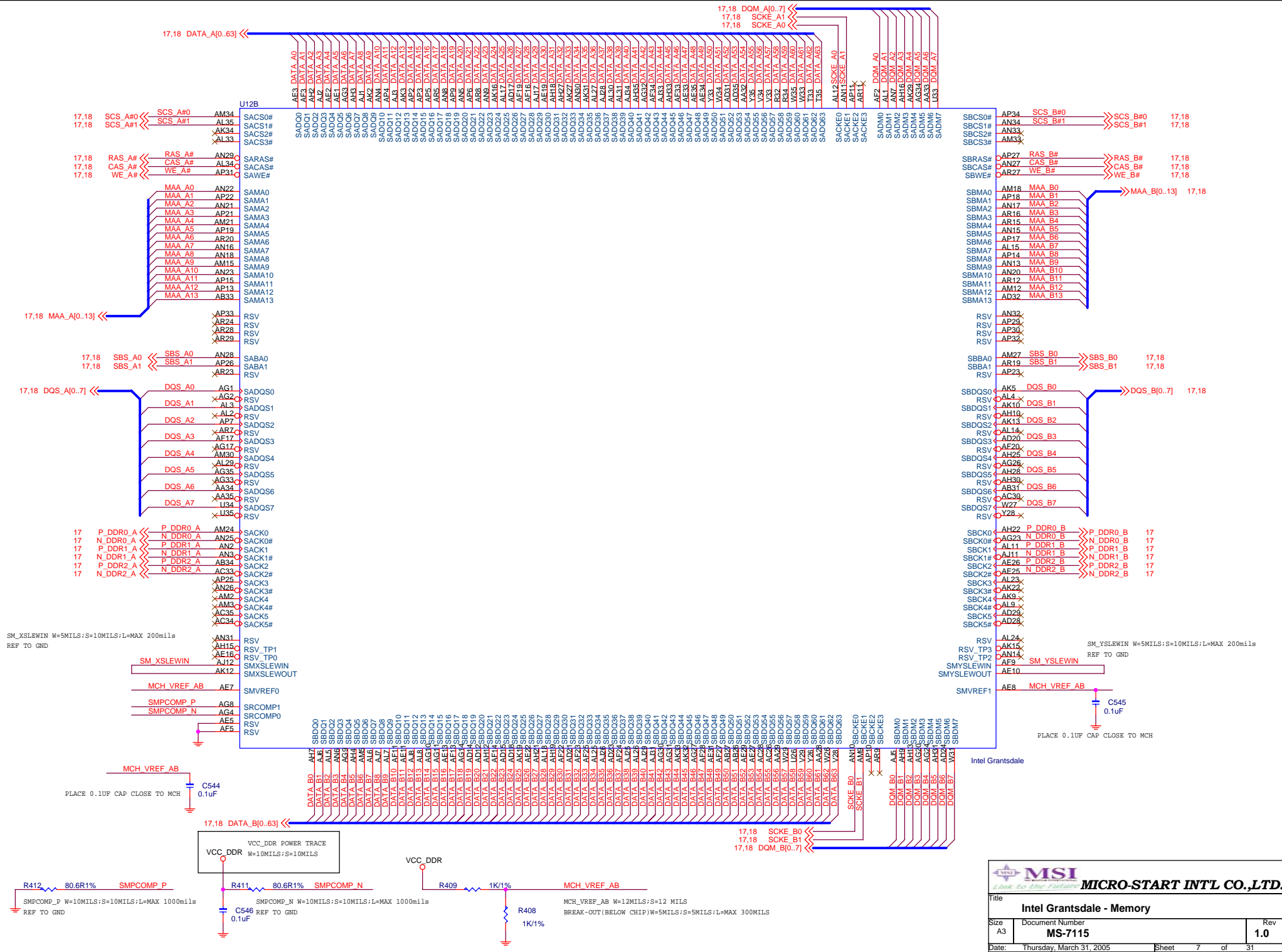
 MICRO-START INT'L CO.,LTD.		
Title COVER SHEET		
Size A3	Document Number MS-7115	Rev 1.0
Date: Thursday, March 31, 2005	Sheet 1	of 31




CPU SIGNAL BLOCK



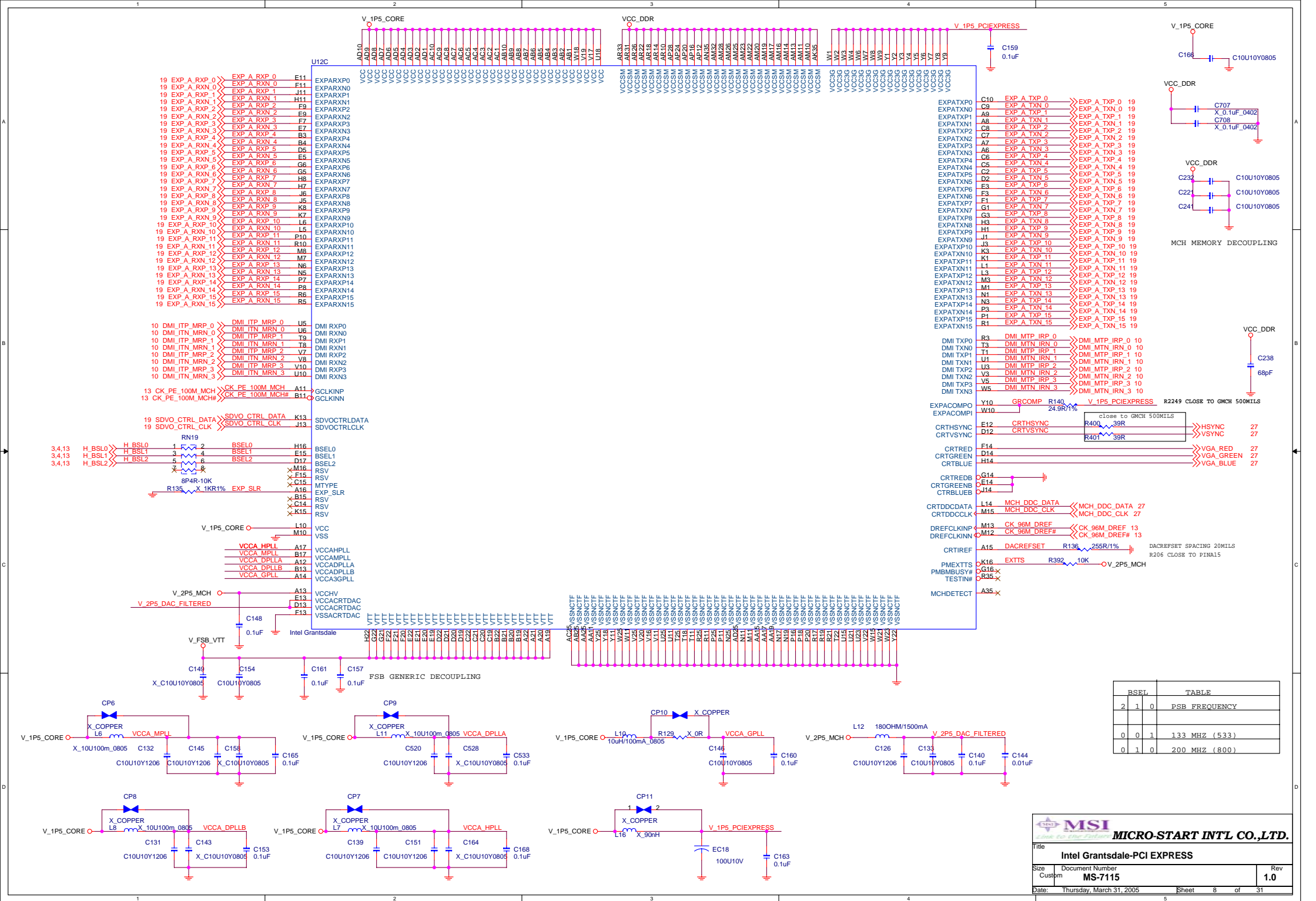




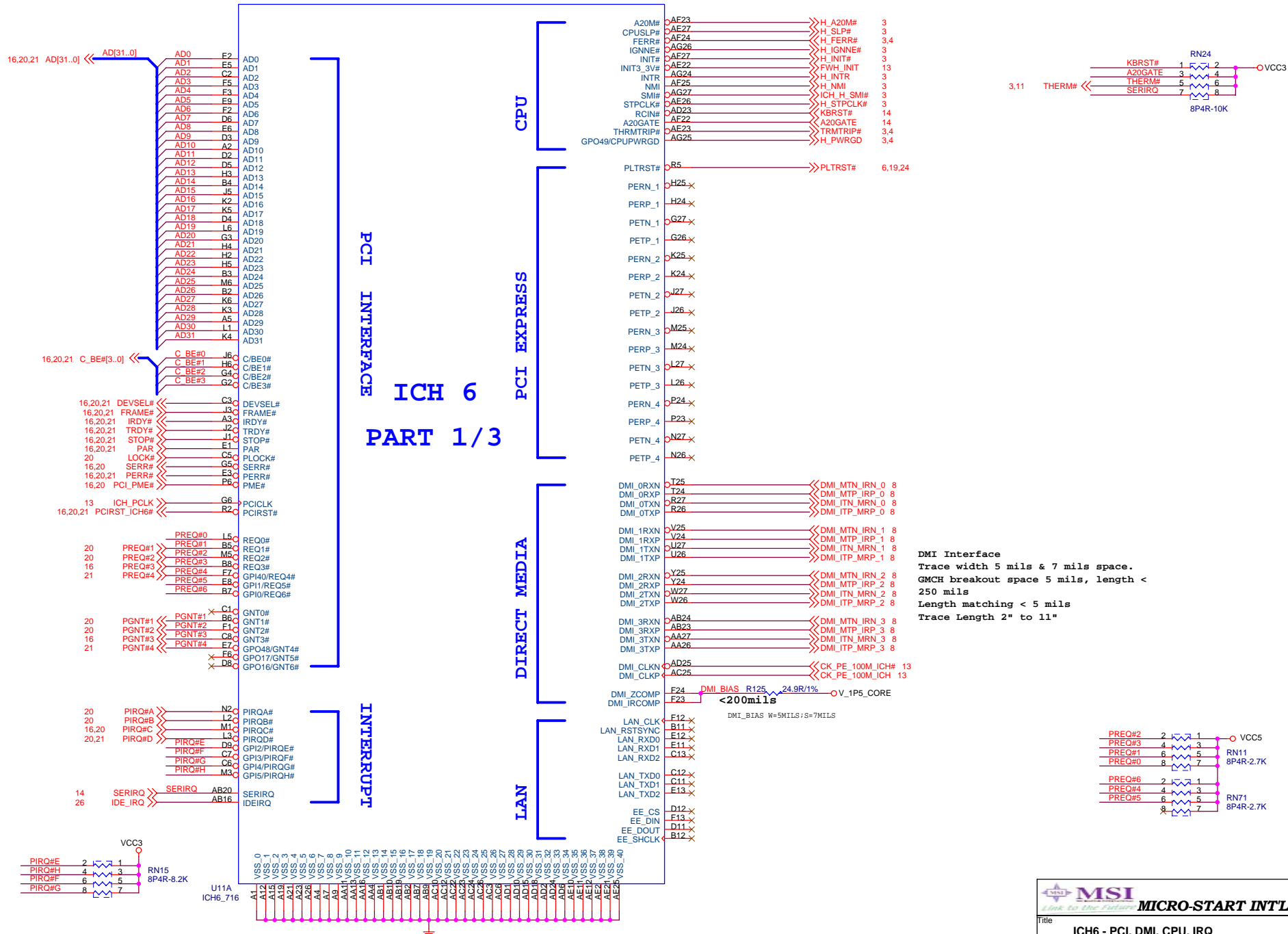
**MICRO-START INT'L CO.,LTD.**

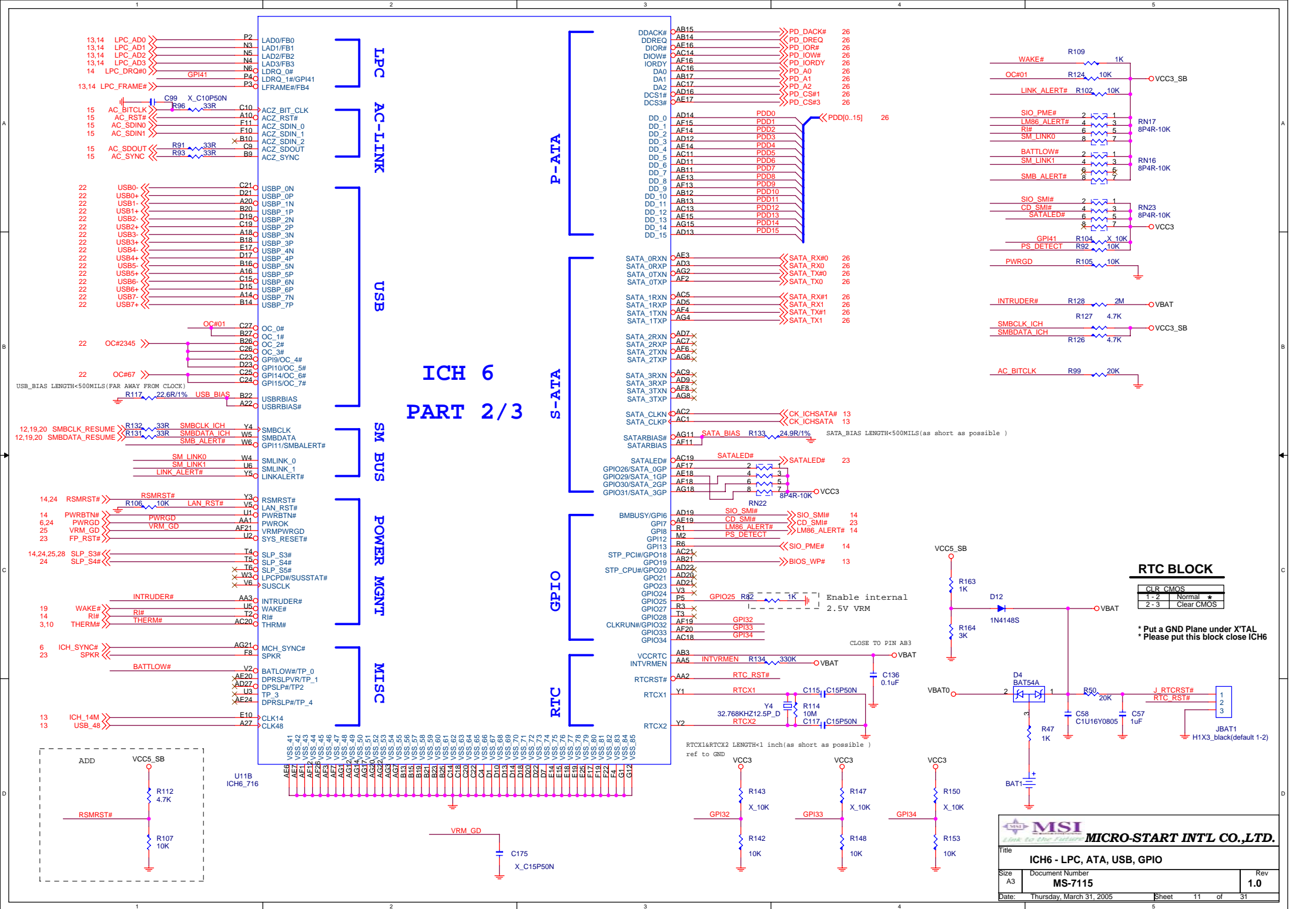
Intel Grantsdale - Memory

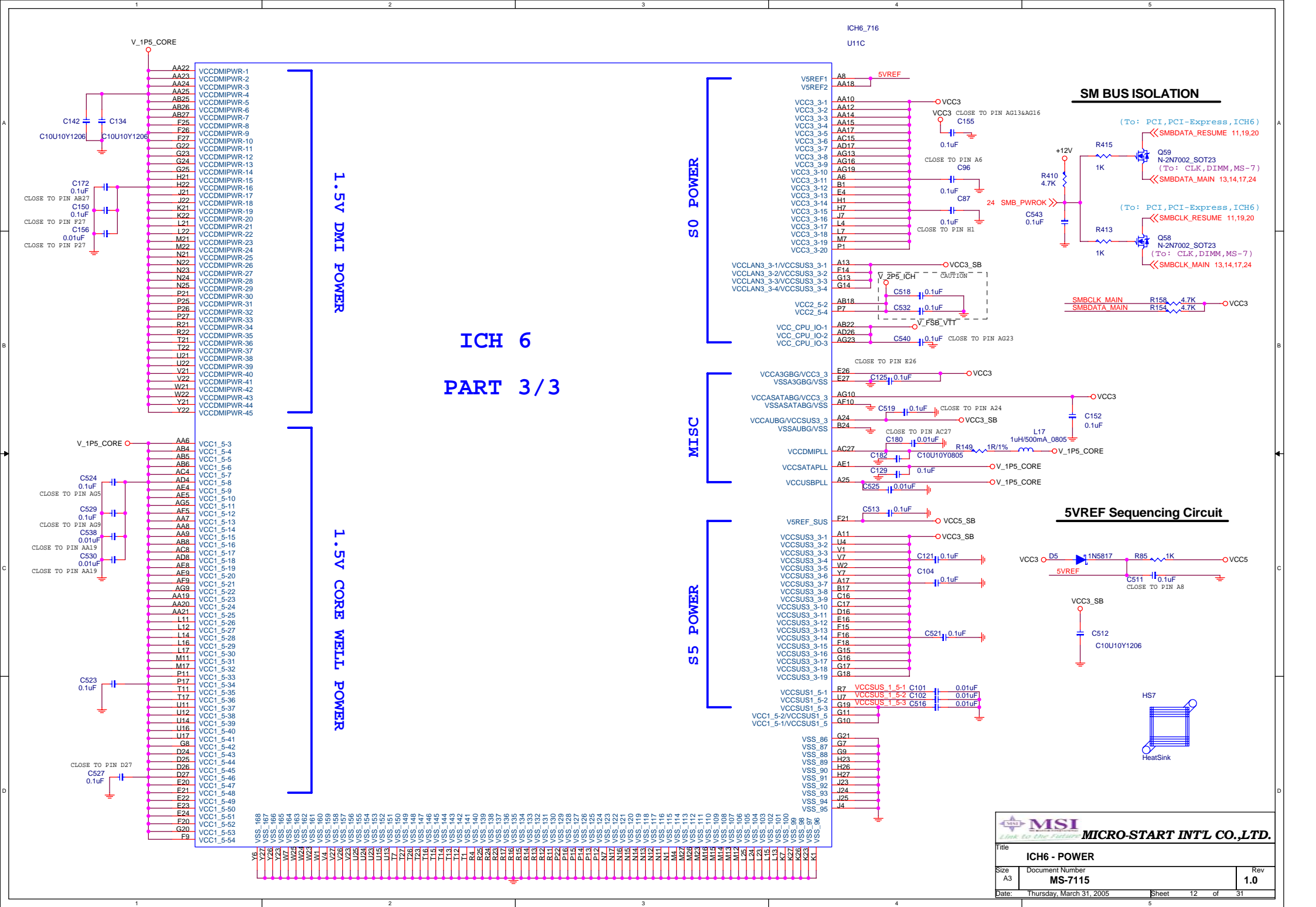
Size A3	Document Number MS-7115	Rev 1.0
Date: Thursday, March 31, 2005	Sheet 7	of 31











[illegible]

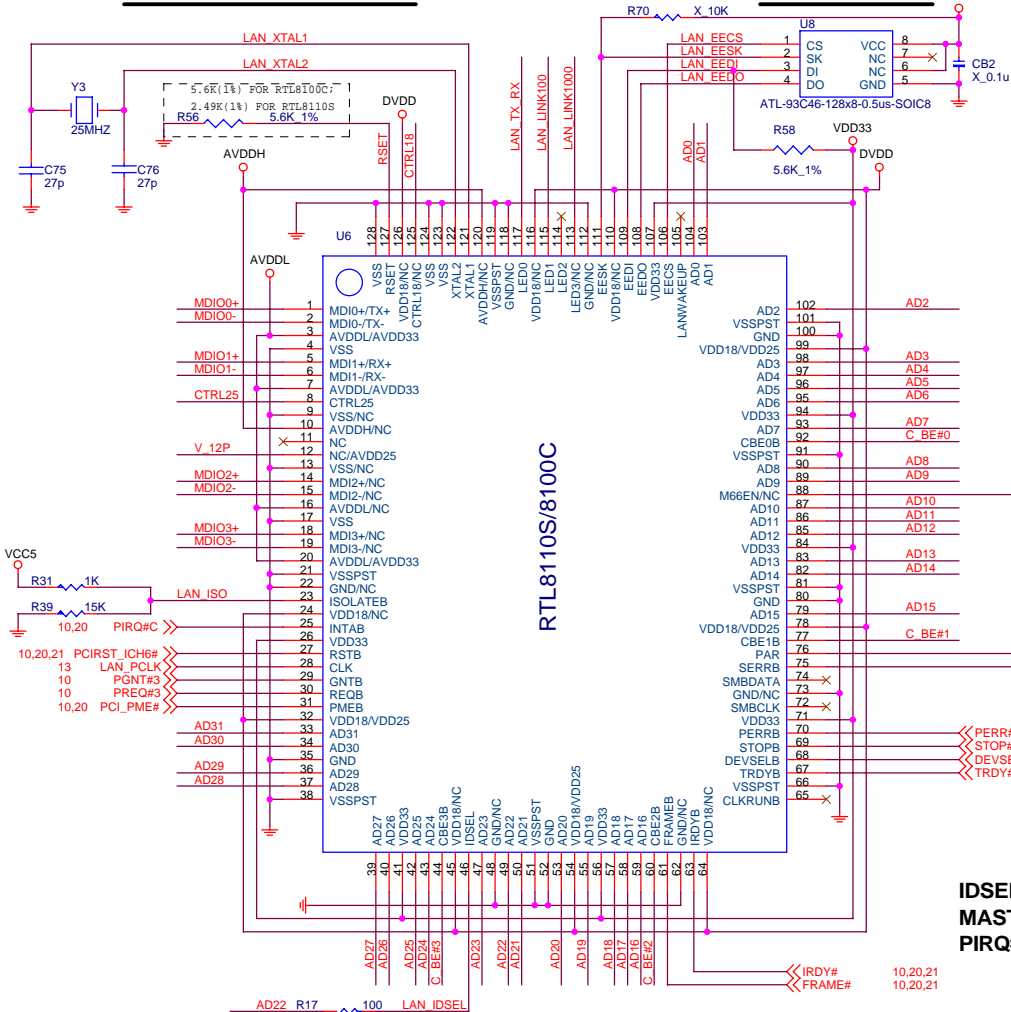
default is high

	RN6	8P4R-1K
BIOS WP#	1	2
PRES1	3	4
PRES2	5	6
PRES3	7	8

VCC3

PCI LAN RTL8110S/8100C

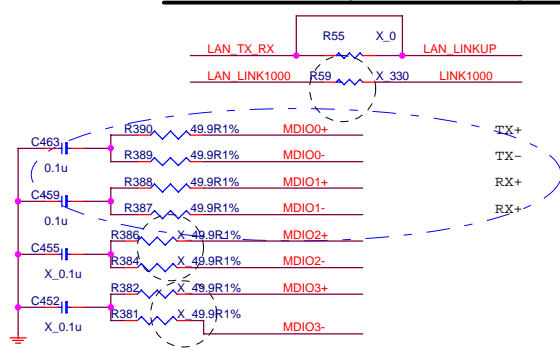
LAN EEPROM



RTL8110S/8100C

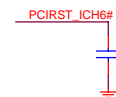
IDSEL = AD29
MASTER = PREQ#3
PIRQ#G

RJ45 Connector (with transformer)

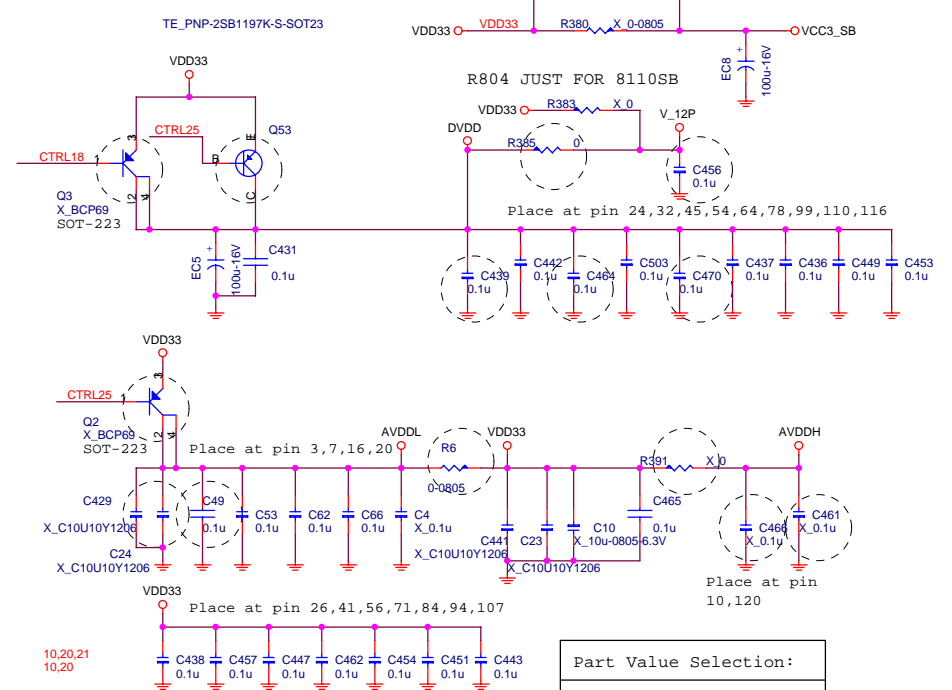


1- MDIO+ & MDIO- pairs should be 100-ohm differential impedance. Route equal length and symmetrically. Separate every pairs.

10,20,21 AD[31..0] >> AD[31..0]
10,20,21 C_BE#[3..0] >> C_BE#[3..0]



DEFAULT 10/100, for GIGALAN OPTION

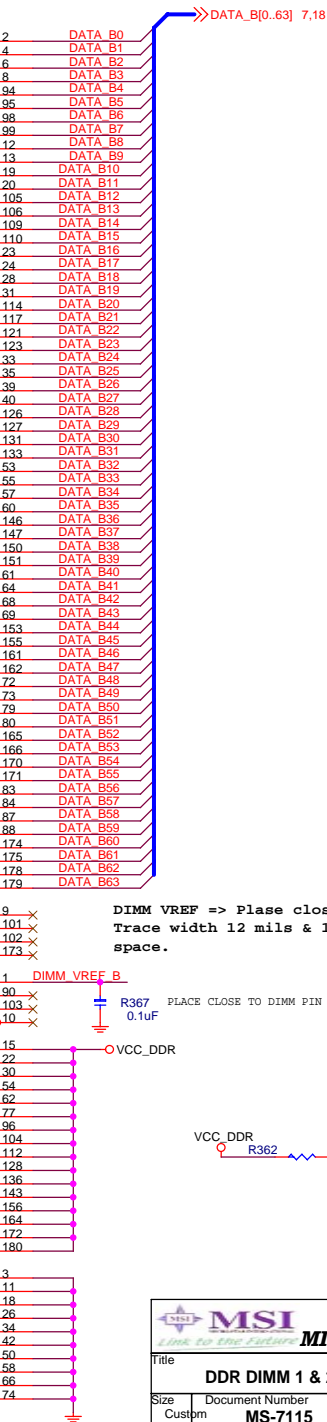
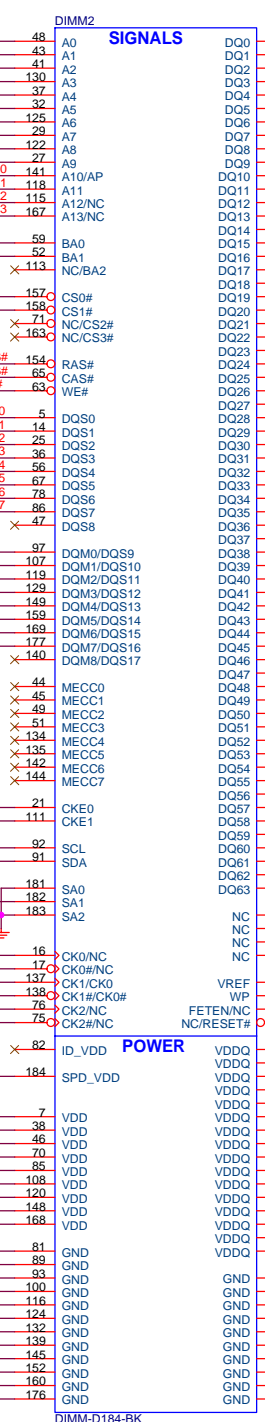


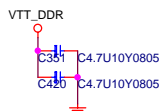
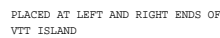
	DVDD	DVDDA	AVDDL	AVDDH	V-12P
8100C	2.5V	2.5V	3.3V	X	2.5V
8110S	1.8V	1.8V	2.5V	3.3V	X

Part Value Selection:
GbE: 8110S LAN(1000M)
TE: 8100C LAN(10/100M)
L: With LAN option
X: No Stuff

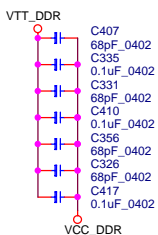
N58-22F0031-S42 for GIGALAN
N58-22F0061-S42 for 10/100

MSI		
Title: REALTEK LAN 8110S/8100C		
Size: A3	Document Number: MS-7115	Rev: 1.0
Date: Thursday, March 31, 2005	Sheet: 16	of 31

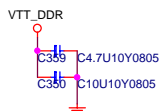
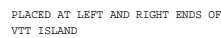
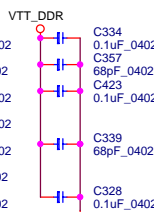
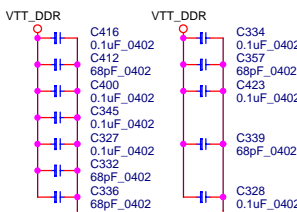




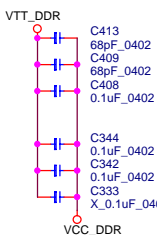
CHANNEL A ADDRESS/CONTROL
STITCHING CAPS



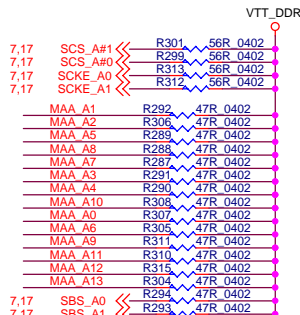
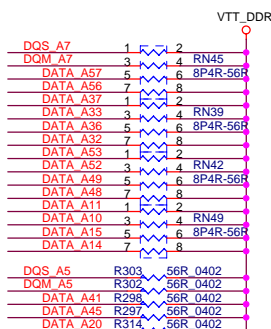
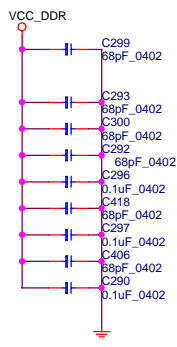
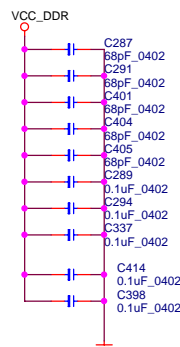
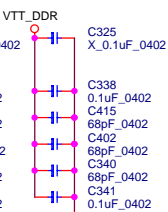
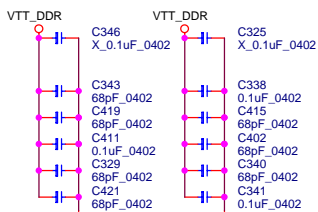
CHANNEL A V_SM_VTT DECOUPLING CAPS



CHANNEL B ADDRESS/CONTROL
STITCHING CAPS



CHANNEL B V SM VTT DECOUPLING CAPS



7,17 WE_A# R296 47R 0402
7,17 RAS_A# R295 47R 0402
7,17 CAS_A# R300 47R 0402

7,17 DQS_A[0..7] << _____

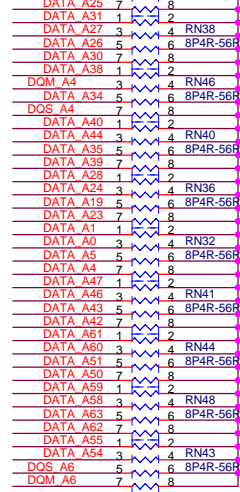
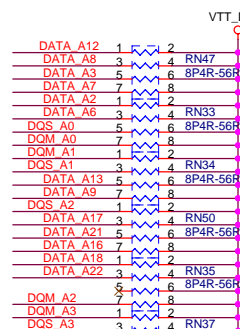
7,17 DATA_A[0..63] << _____

7,17 DQM_A[0..7] <<

Data Group: SDQS,SDQ & SDM (56 ohm)

Control Group: SCS# & SCKE (56 ohm)

Command Group: SMA,SBS,SRAS#SCAS# & SWE# (47 ohm)



7,17 WE_B# R354 47R 0402
7,17 RAS_B# R353 47R 0402
7,17 CAS_B# R357 47R 0402

7,17 DQS_B[0..7] <<—

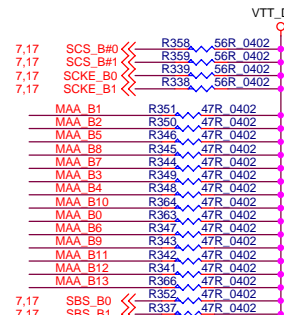
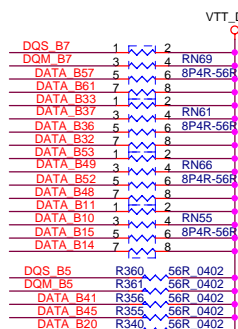
7.17 DATA_B[0..63] <<—

7,17 DQM_B[0..7] <<

Data Group: SDQS,SDQ & SDM (56 ohm)

Control Group: SCS# & SCKE (56 ohm)

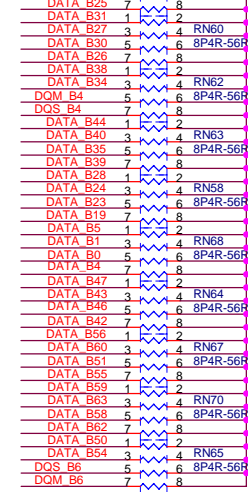
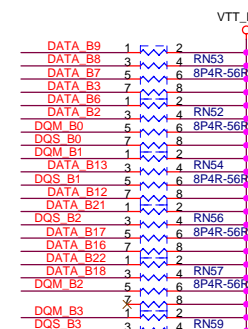
Command Group: SMA,SBS,SRAS#SCAS# & SWE# (47 ohm)



7,17 WE_B# R354 47R 0402
7,17 RAS_B# R353 47R 0402
7,17 CAS_B# R357 47R 0402

7,17 DQS_B[0..7] <<—

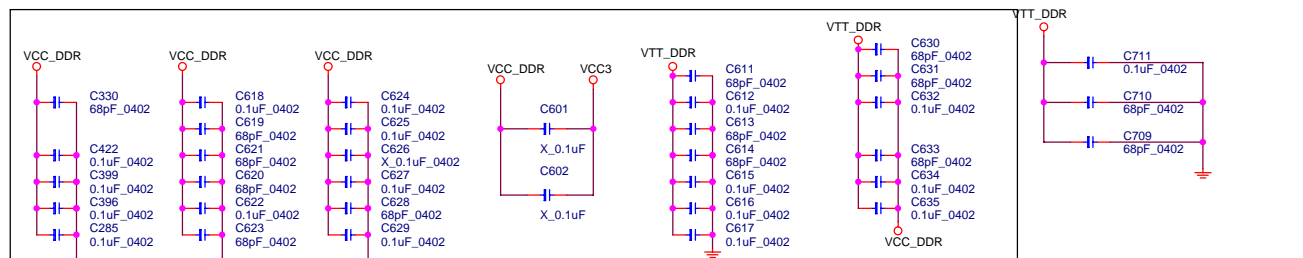
7,17 DQM_B[0..7] <<—



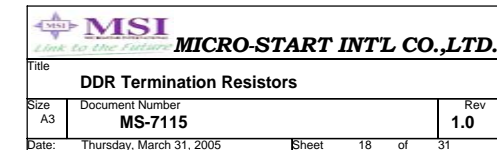
SDM (56 ohm)

SCKE (56 ohm)

,SRAS#SCAS# & SWE# (47 ohm)

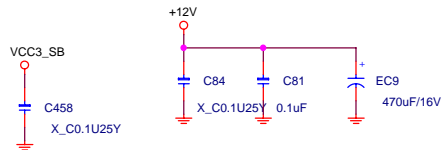
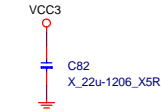
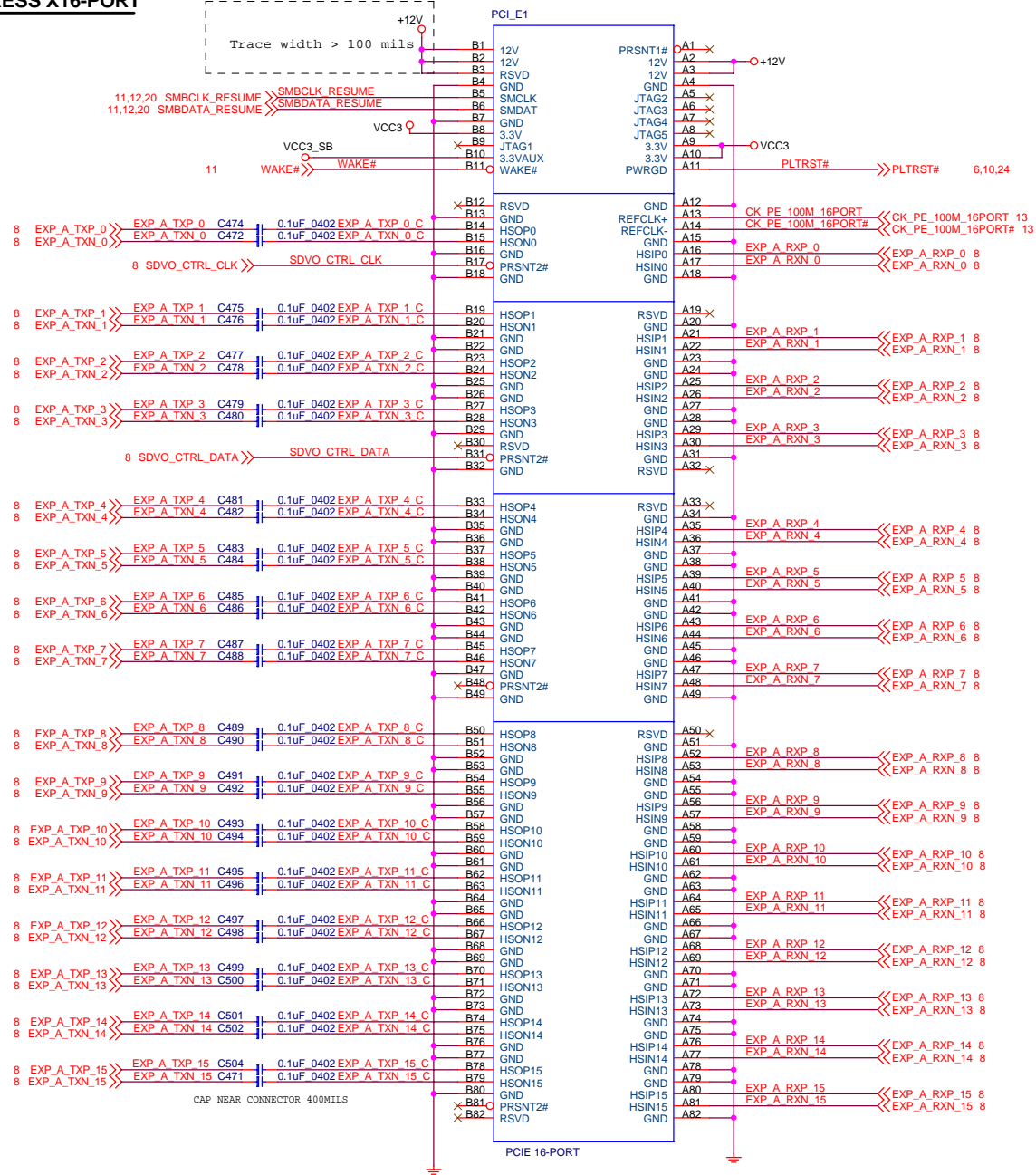


FOR EMI

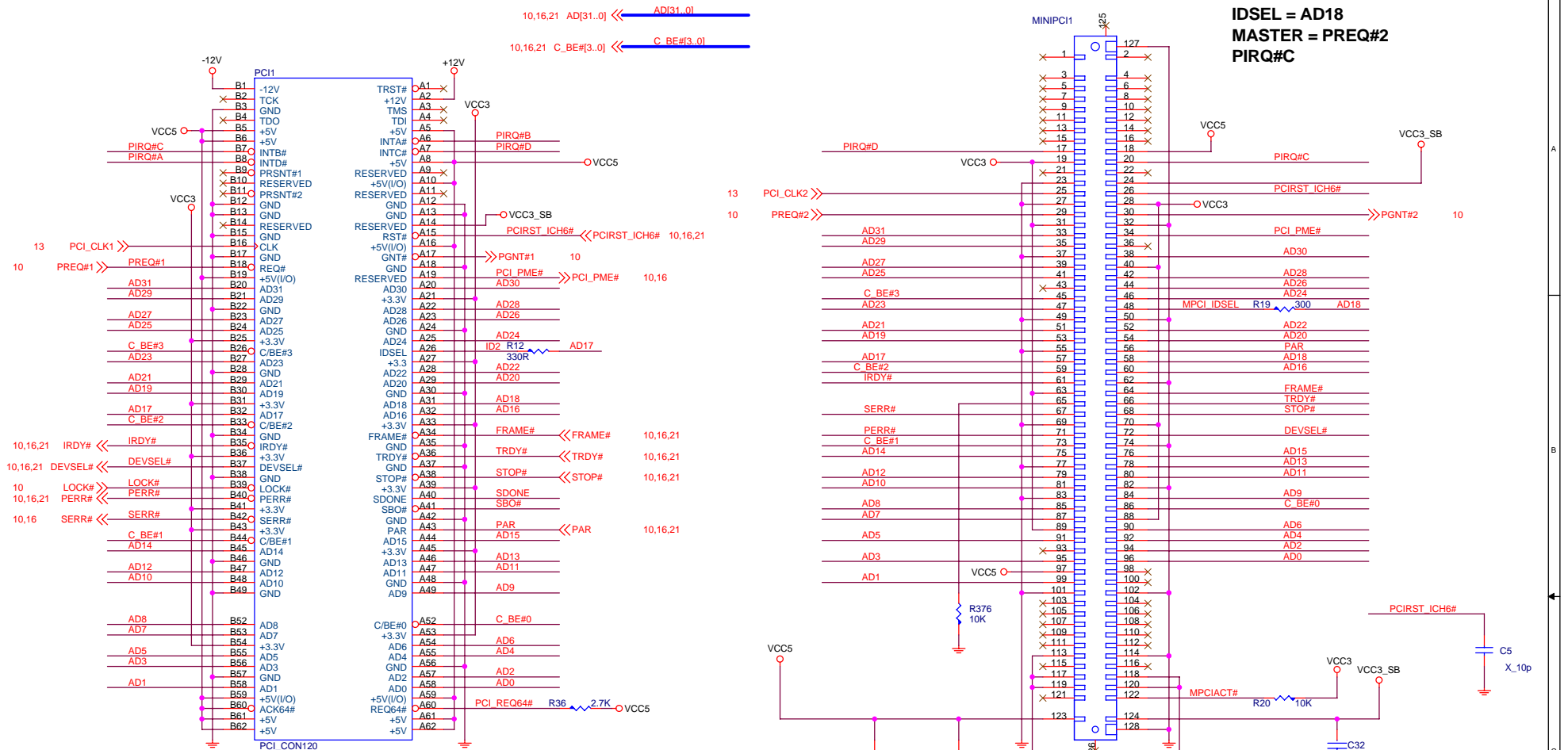


Title			
DDR Termination Resistors			
Size	Document Number	Rev	
A3	MS-7115	1.0	
Date:	Thursday, March 31, 2005	Sheet	18 of 31

PCI EXPRESS X16-PORT



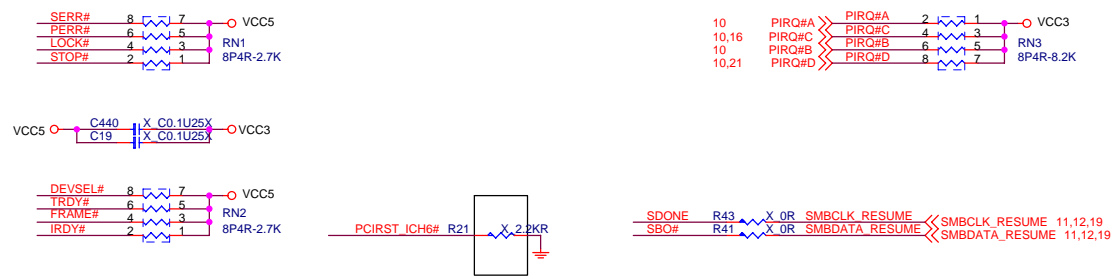
MICRO-START INT'L CO.,LTD.		
Title		
PCI-Express X16 Port		
Size	Document Number	Rev
A3	MS-7115	1.0
Date:	Thursday, March 31, 2005	Sheet 19 of 31



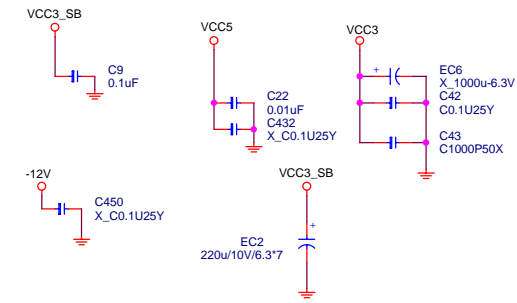
ISEL = AD18
MASTER = PREQ#2
PIRQ#C


ISEL = AD17
MASTER = PREQ#1
PIRQ#B

PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS

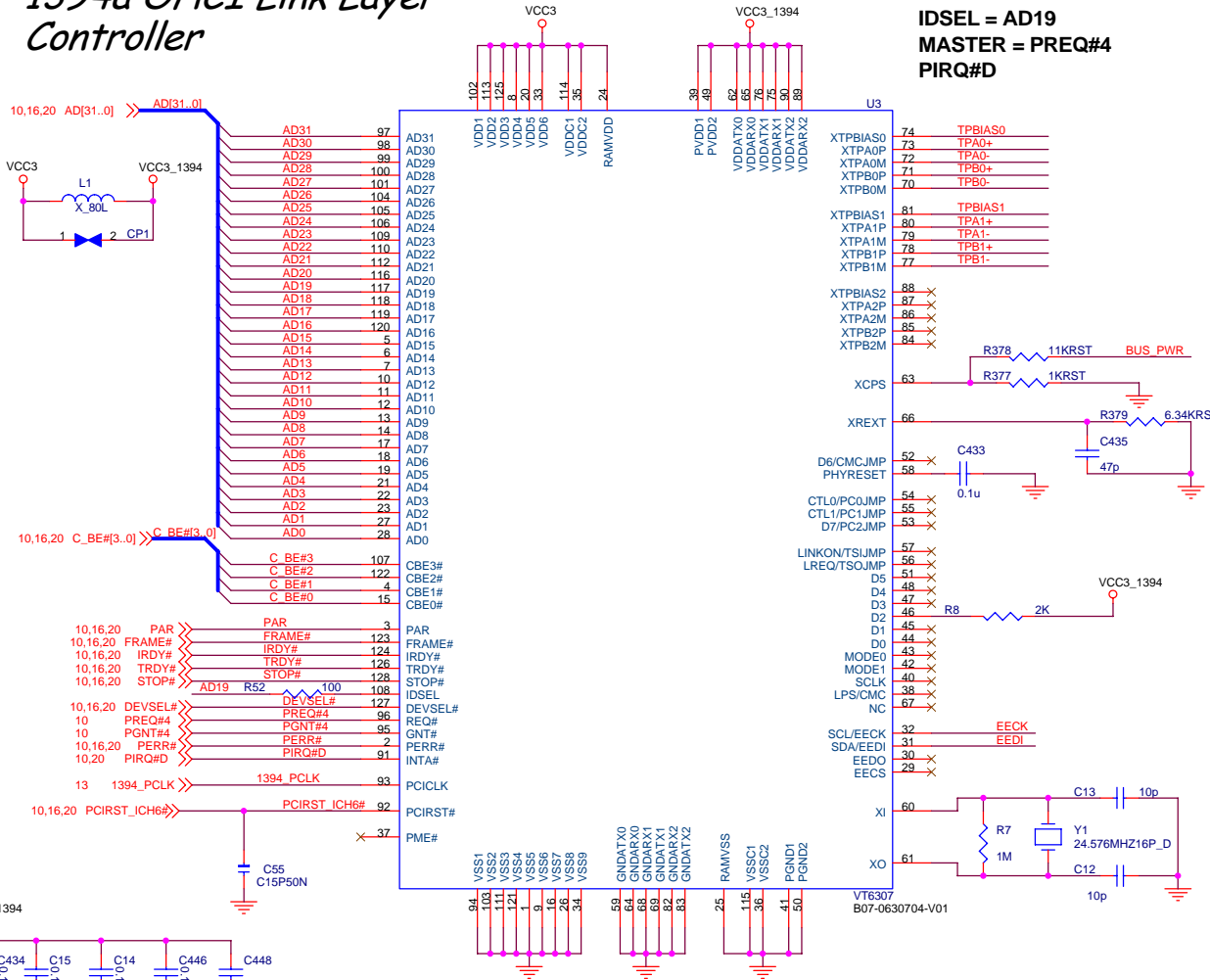




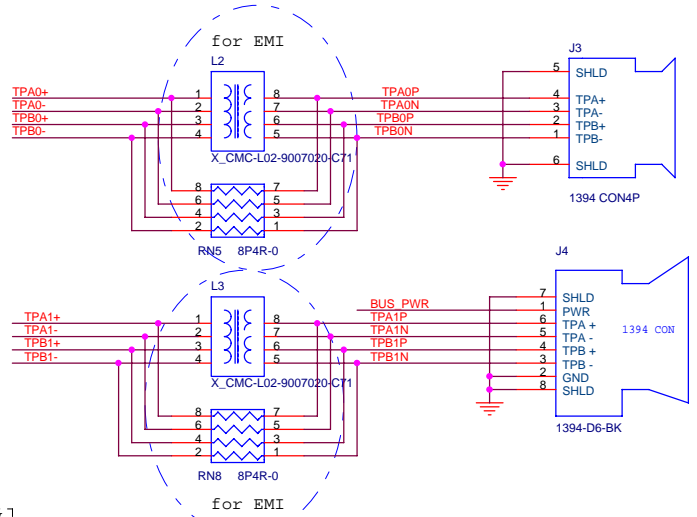
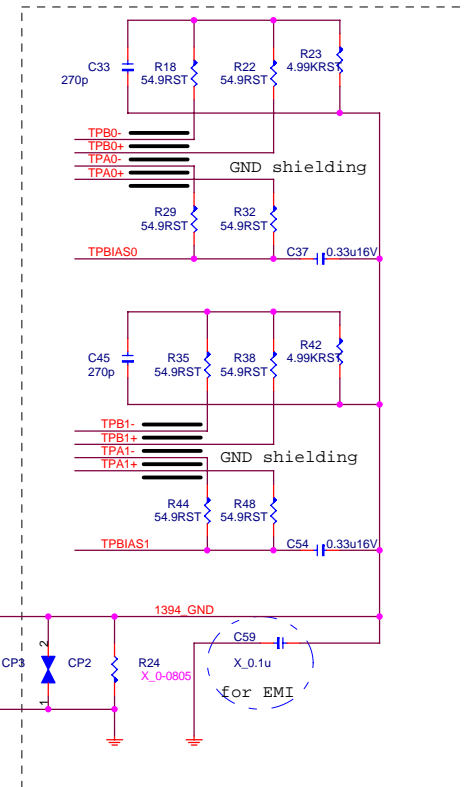
MICRO-START INT'L CO.,LTD.

Title PCI Slot&MINI PCI		
Size A3	Document Number MS-7115	Rev 1.0
Date: Thursday, March 31, 2005	Sheet 20	of 31

1394a OHCI Link Layer Controller



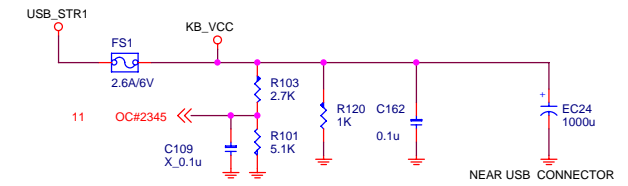
IDSEL = AD19
MASTER = PREQ#4
PIRQ#D



[25V/CAP: EC80 NP: C93-1012511-G01 FP: 100U_16V]

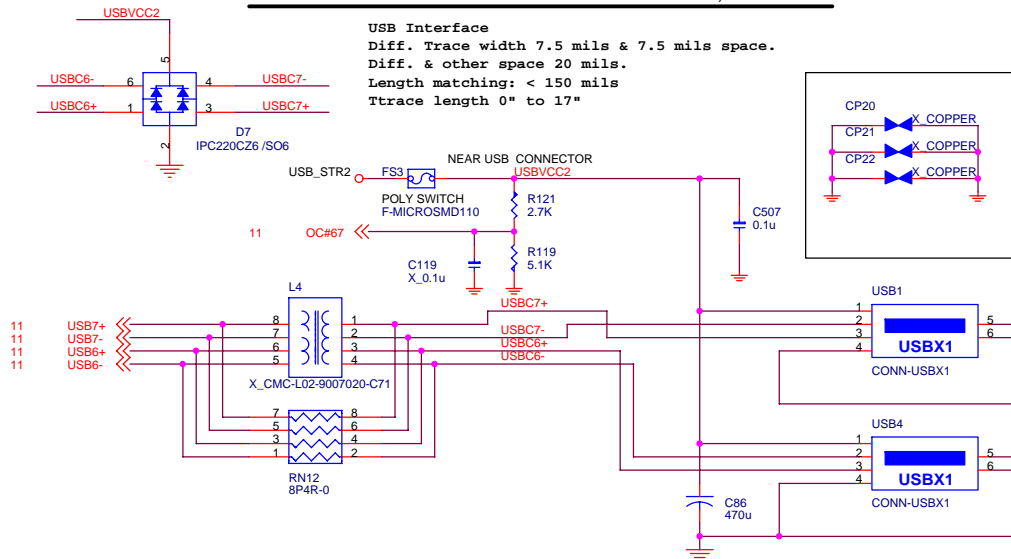
MICRO-STAR INT'L CO., LTD.			
Title IEEE 1394			
Size	Document Number MS-7115		Rev 1.0
Date:	Thursday, March 31, 2005	Sheet	21 of 31

POWER CIRCUIT FOR USB PORT 1~4



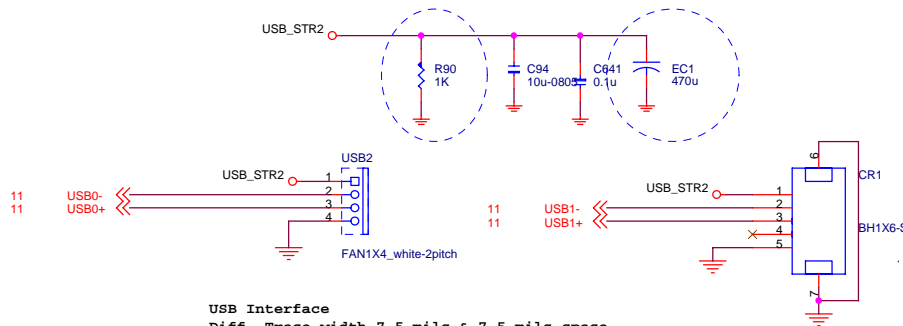
FRONT USB CONNECTOR FOR USB PORT 6,7

USB Interface
Diff. Trace width 7.5 mils & 7.5 mils space.
Diff. & other space 20 mils.
Length matching: < 150 mils
Ttrace length 0" to 17"



MCE IR CONNECTOR

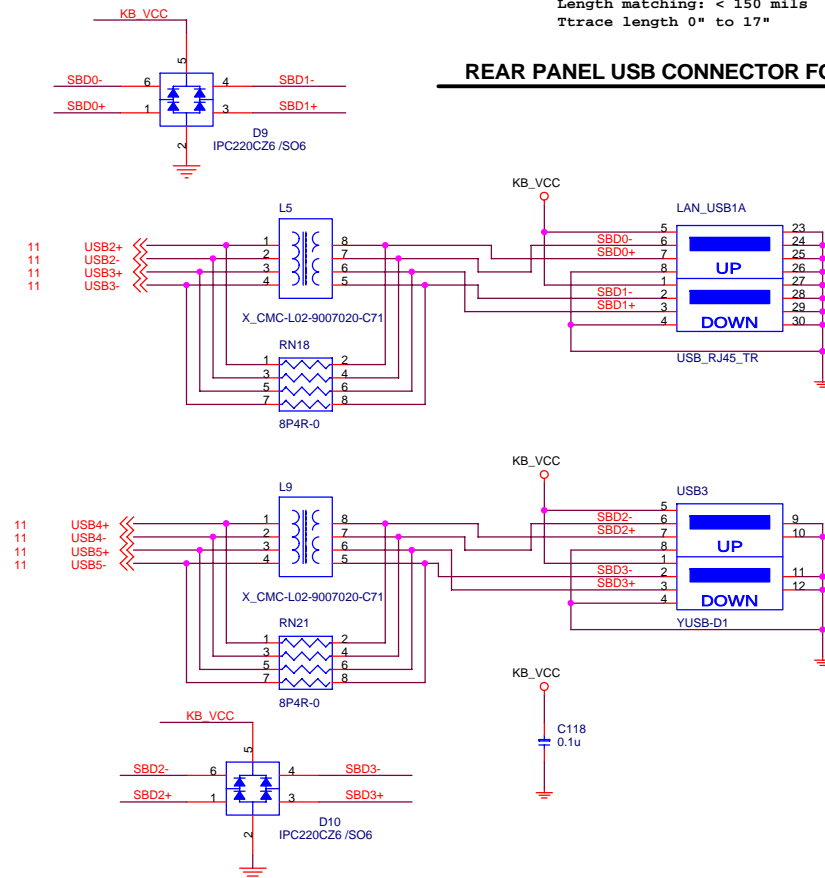
FRONT CARD READER USB CONNECTOR



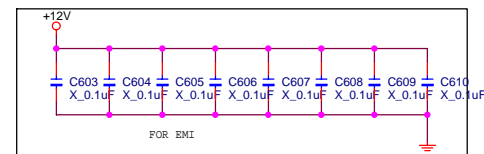
USB Interface
Diff. Trace width 7.5 mils & 7.5 mils space.
Diff. & other space 20 mils.
Length matching: < 150 mils
Ttrace length 0" to 17"

REAR PANEL USB CONNECTOR FOR USB PORT 1~4

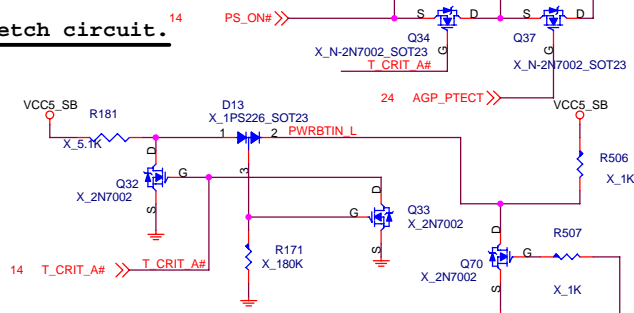
USB Interface
Diff. Trace width 7.5 mils & 7.5 mils space.
Diff. & other space 20 mils.
Length matching: < 150 mils
Ttrace length 0" to 17"



ATX Connector

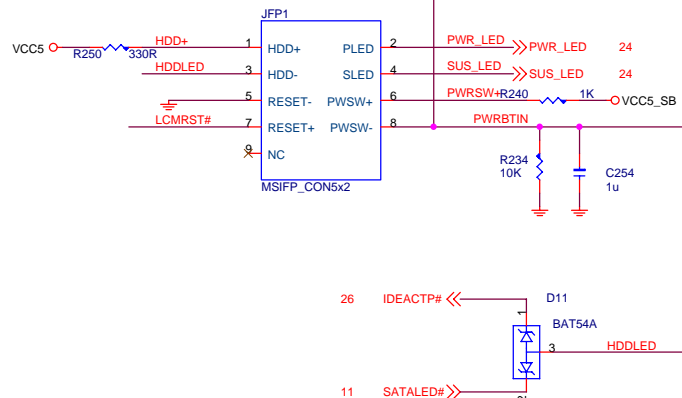


Latch circuit.



(Put at Solder Side)

Intel Front Panel



FOR EMI

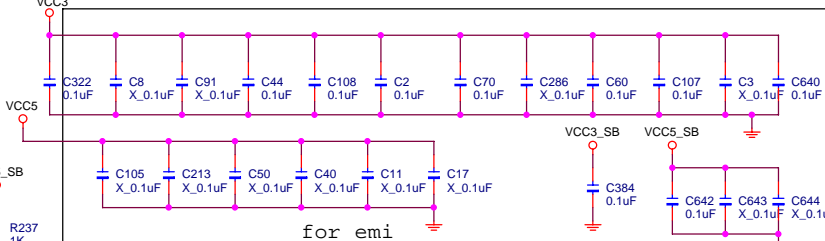
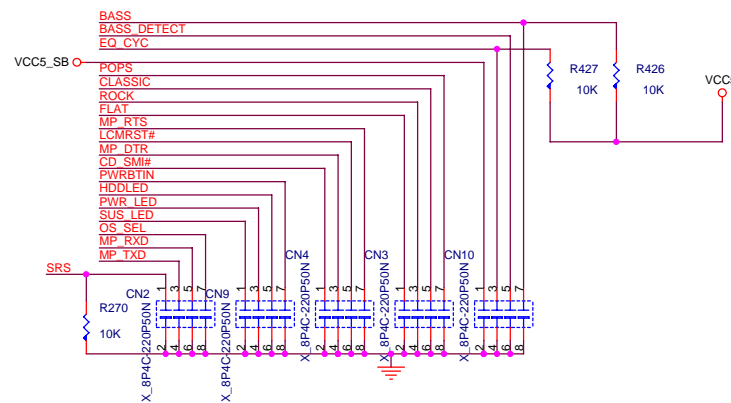
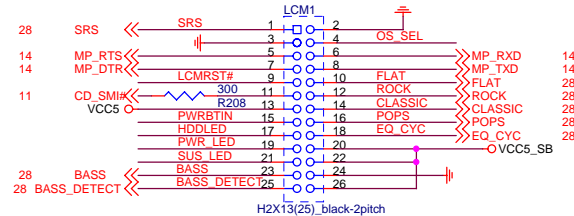
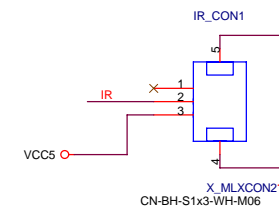


Table for POWER LED's behavior on LCM.

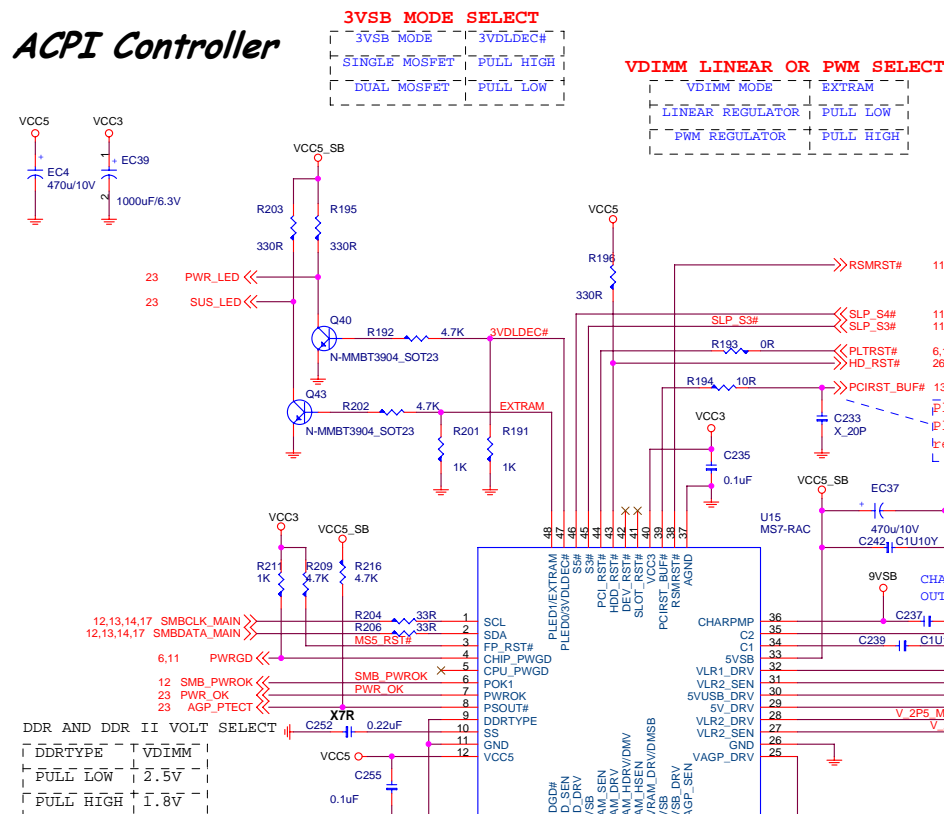
MODE	LCM 1	PLED1 PIN19	PLED2 PIN21	LED State
S0/ INSTANT-ON		H	L	Green
S1		Flash	L	Flash Green / 1Hz
S3		L	H	Yellow
S4/5		L	L	Dark



IR Connector



ACPI Controller

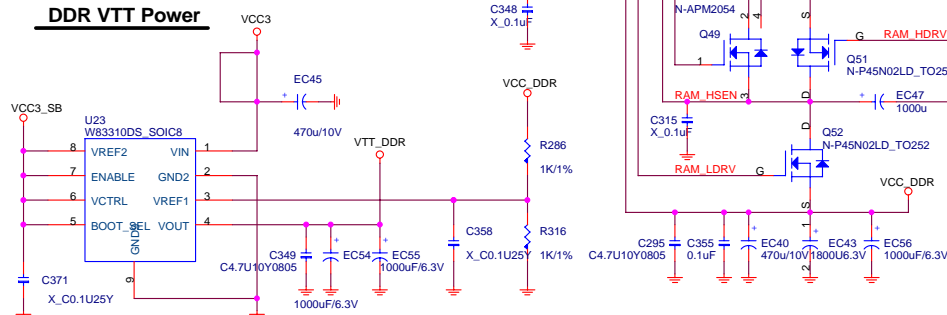


THIS PIN IS OPEN DRAIN OUTPUT

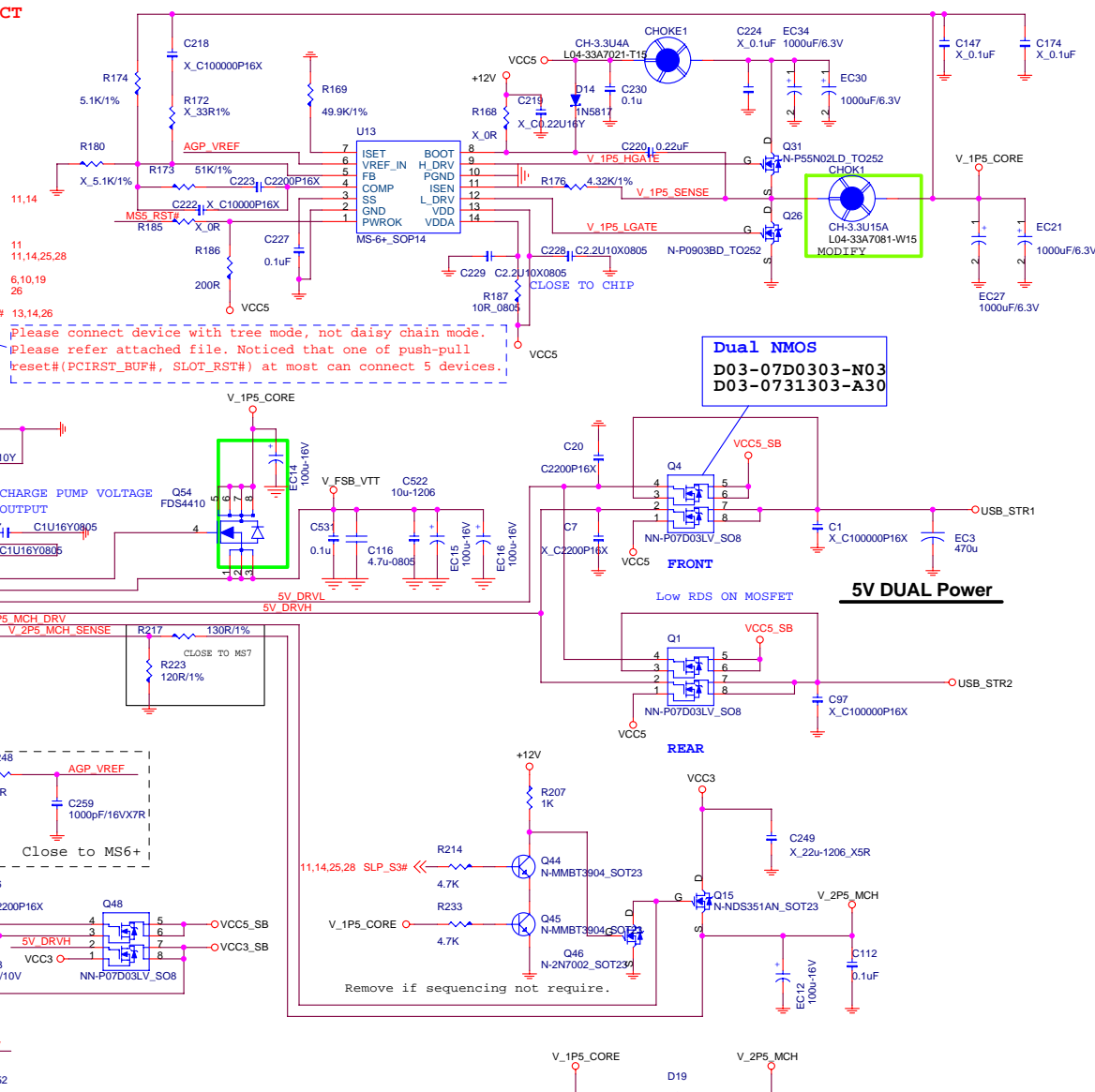
VCC VID / VID GOOD

Place MOSFET near CPU

DDR VTT Power

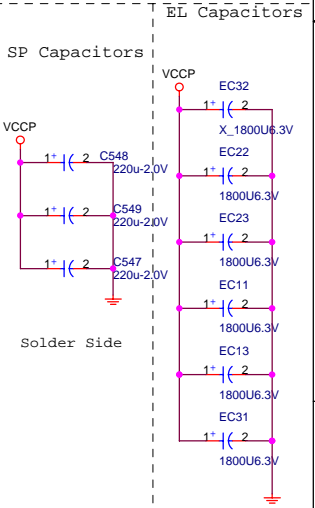
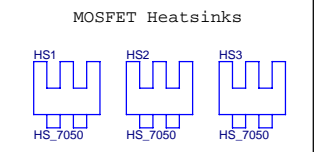
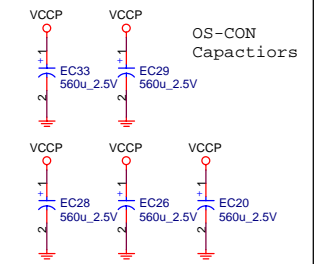
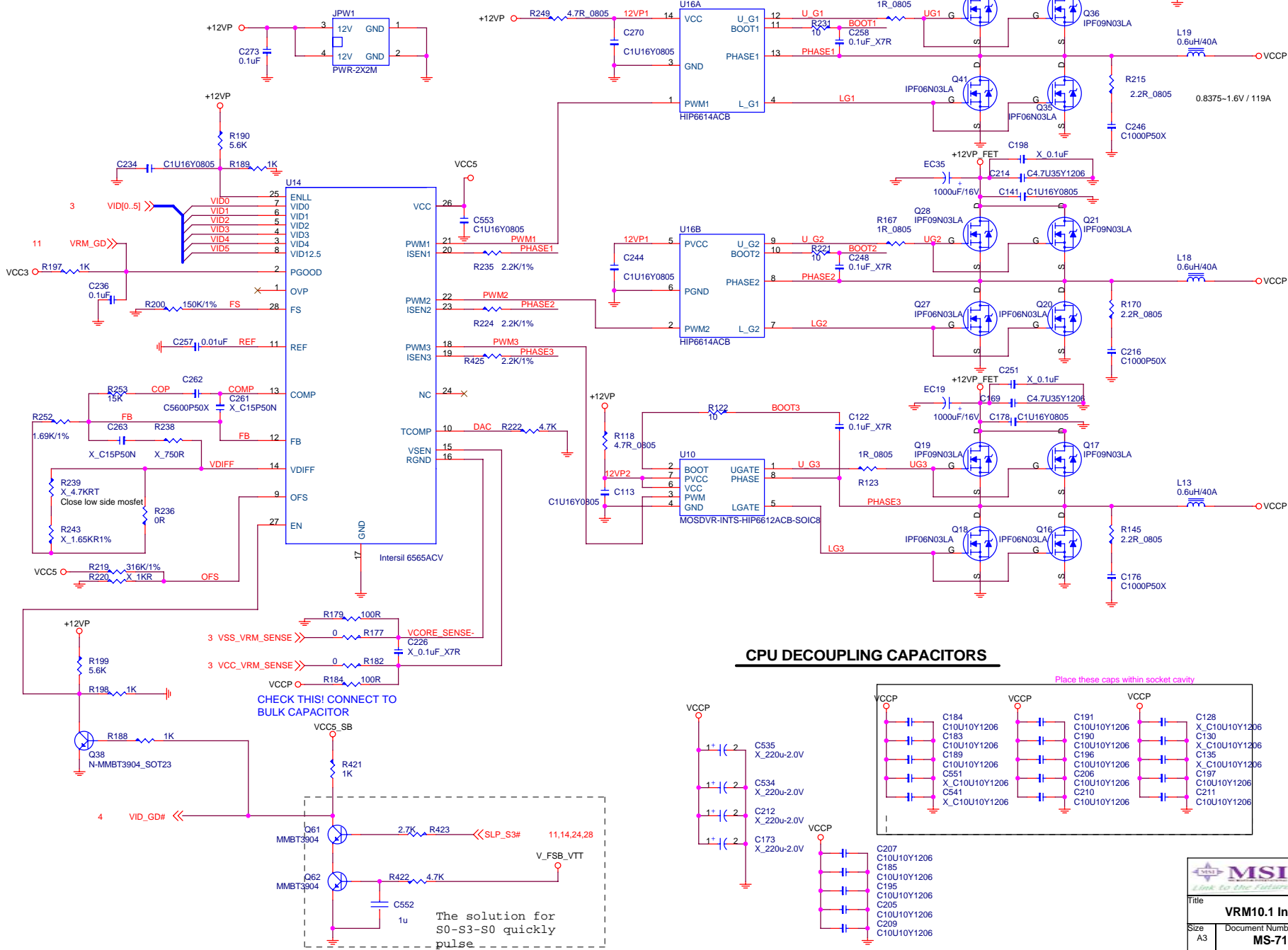


AGP POWER

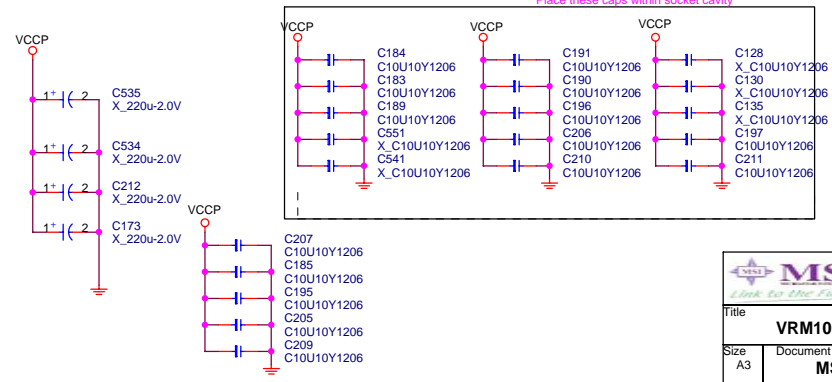


Voltage Regular Module

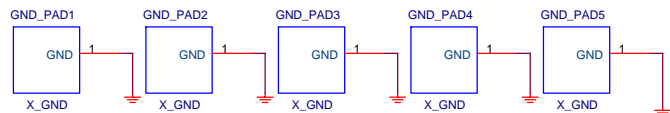
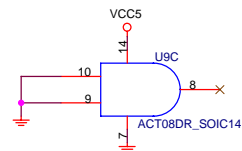
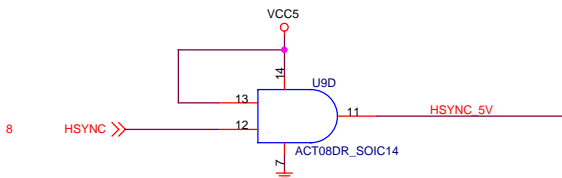
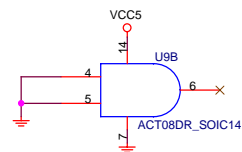
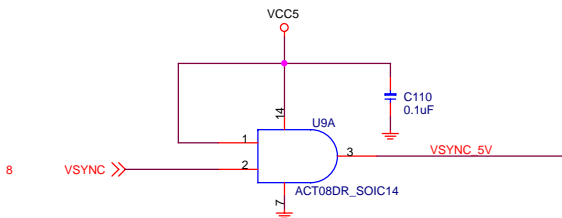
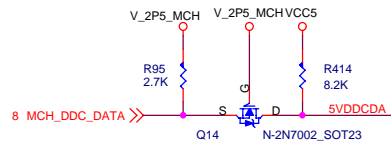
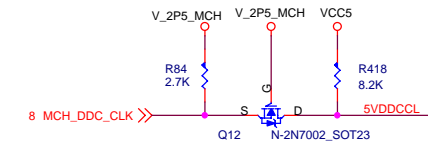
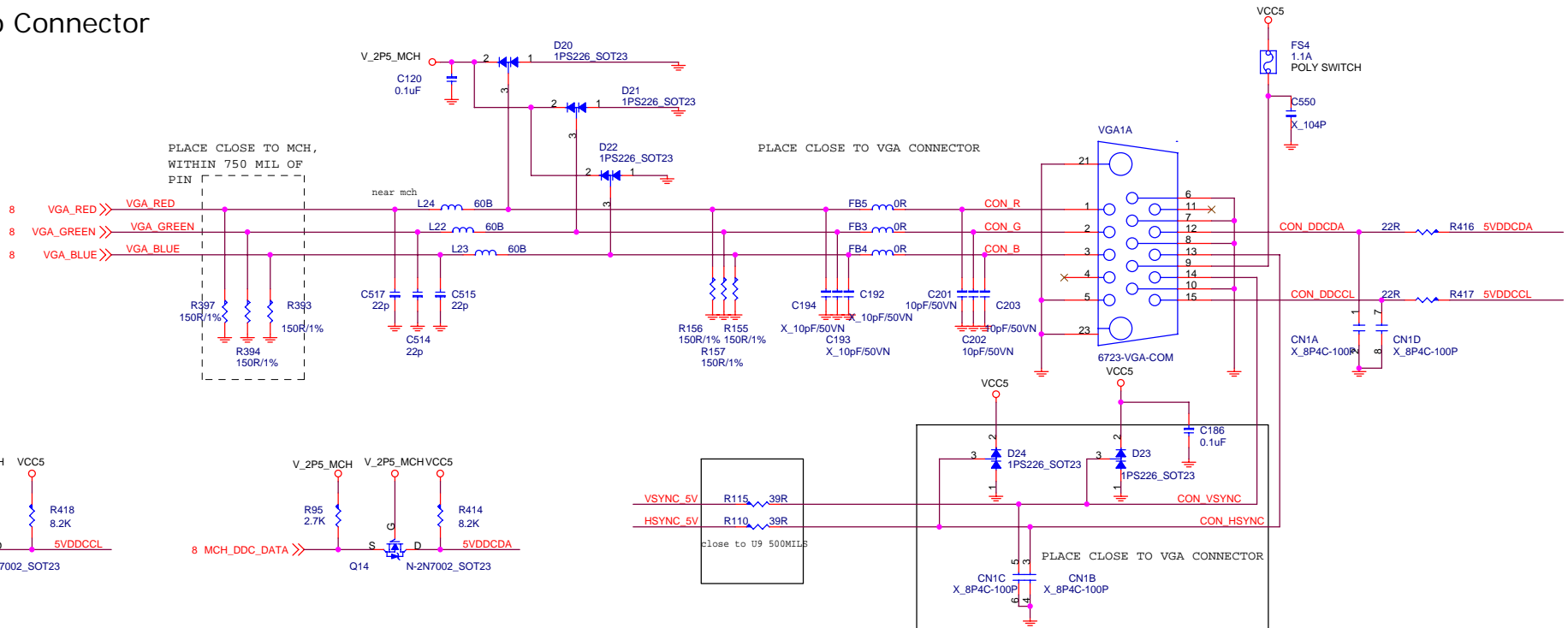
MOSFET Gate signal : 20 mils
Phase signal : 20 mils
Boot signal : 16 mils



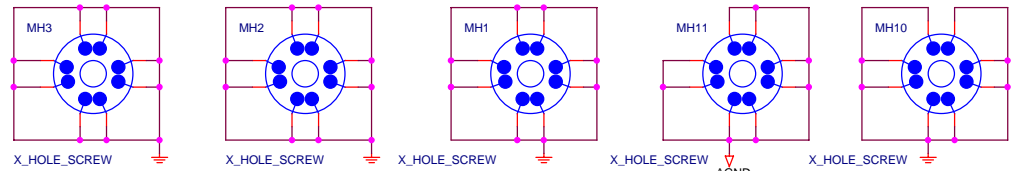
CPU DECOUPLING CAPACITORS



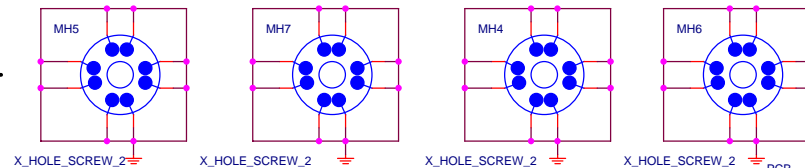
Video Connector



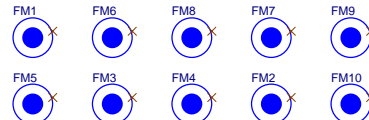
Mounting Holes



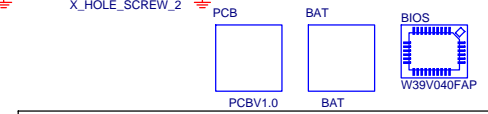
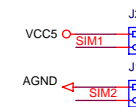
CPU Hole



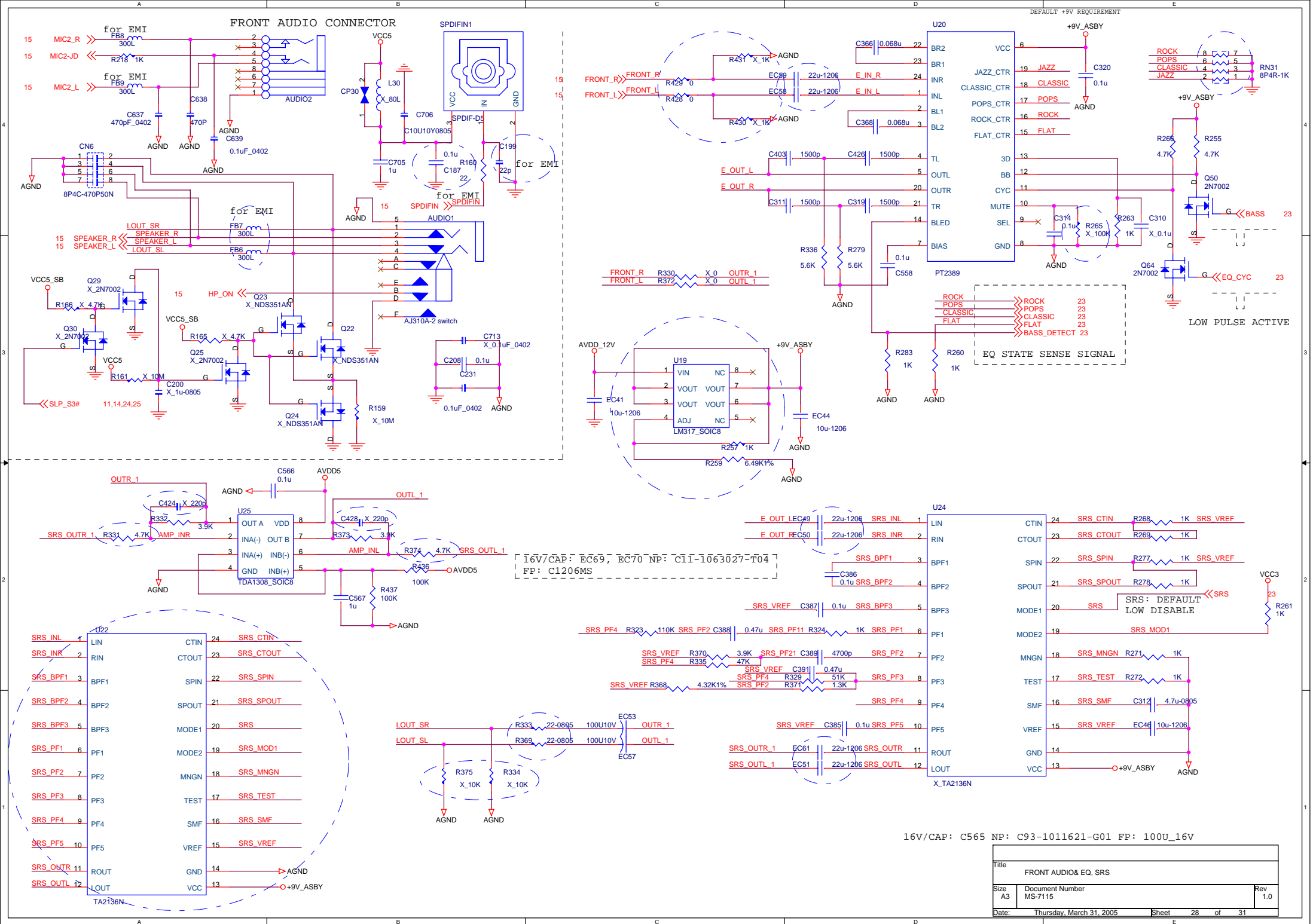
Optics Orientation Holes



Simulation



MSI <i>Link to the Future</i>		
MICRO-START INT'L CO.,LTD.		
VGA CON&Misc		
Size A3	Document Number	Rev
	MS-7115	1.0
Date: Thursday, March 31, 2005	Sheet 27 of 31	



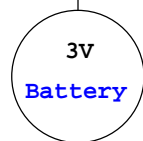
PRESCOTE		
0.8375V - 1.6000V Core	-	95A
1.2V FSB Vtt	-	2.9~3.5 A

Gransdale GMCH		
1.2V FSB Vtt	-	1.0A
2.6V DDR I/O (S0,S1)	-	3.0A
2.6V DDR I/O (S3)	-	250mA
*2.5V DAC	-	0.07A
2.5V HV	-	5mA
1.5V Core (Integrated)	-	9.7A
1.5V Core (Discrete)	-	7.7A
*1.5V PCI Express	-	1.4A

ICH6		
1.2V VCC_CPU	-	14mA
1.5V Core	-	1.88A
*1.5V PCI Express	-	560mA
1.5V SATA	-	430mA
+3.3V VccSus	-	330mA
RTC (G3)	-	5uA
5VRef	-	1mA
5VrefSus	-	10mA
+3.3V	-	220mA

FWH		
+3.3V (S0,S1)	-	107mA

CLOCK GEN:+3.3V 560mA
 SUPERIO:+3.3V:50mA;3.3SBY:50mA
 AUDIO:3.3V:30mA;5V:100mA
 LAN:3.3SBY:400mA
 1394:3.3V:160mA(BUS PWR+12V:1.4A)
 MS7:5VSB:350mA;3.3V:100mA



ISL6556		
VCCP	VRM 10.1	
0.8375V-1.6000V	95A	
4-Phase Switch		

W83310DS		
VTT_DDR		
1.3V Linear	1.0A	

MS7 Regulator		
V_FSB_VTT		
1.2V Linear	4.6A	
VCC_DDR		
2.6V (S0,S1)	7.0A	
Linear(S3)	570mA	
V_2P5_MCH		
2.5V Linear	100mA	
VCC3_SB		
3.3V Linear	1.5A	
5VDUAL1,2		
5V Linear	22mA	

MS6+ Regulator		
V_1P5_CORE		
1.5V Switch	14A	

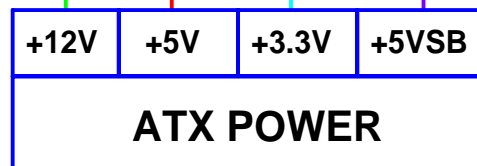
DDR DIMM & TERMINATOR		
1.3V VTT_DDR	-	1.0A
2.6V VCC_DDR (S0,S1)	-	4.0A
2.6V VCC_DDR (S3)	-	160mA

PCI Express x16 slot		
+12V	-	4.4 A
+3.3Vaux (wake)	-	375mA
+3.3Vaux (no wake)	-	20mA
+3.3V	-	3.0A

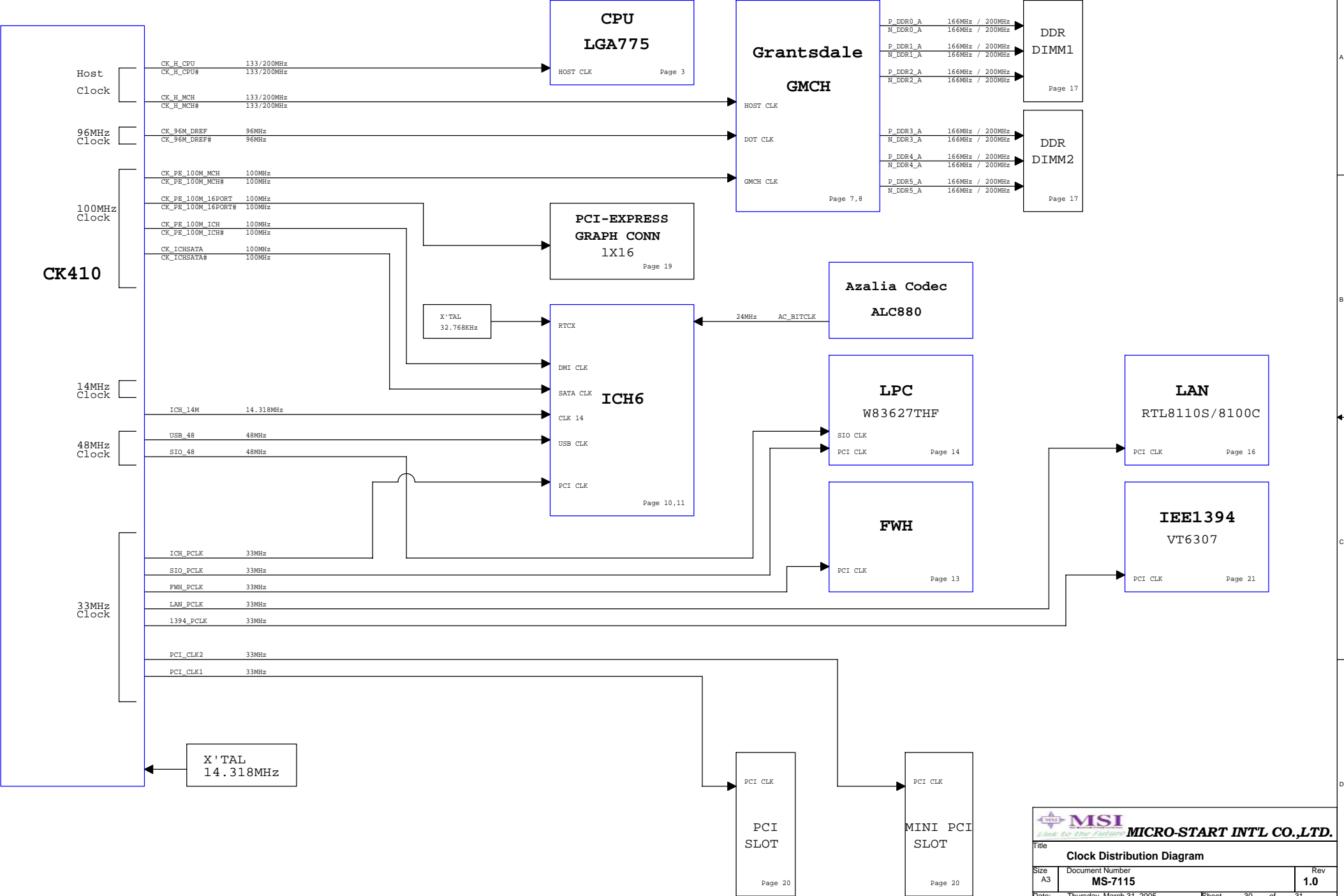
PCI slot x1&mini pci		
+3.3Vaux (wake)	-	375mA
+3.3Vaux (no wake)	-	20mA
+3.3V	-	7.6A
+5V	-	5.0A
+12V	-	0.5A

USB		
+5V (S0,S1)	-	4A
+5V (S3)	-	20mA

PS2		
+5V (S0,S1)	-	345mA
+5V (S3)	-	2.0mA



Clock Distribution Diagram



SCHEMATIC HISTORY

Rev	Date	Page	Description
0A	2005/01/21	14	W83627THF voltage monitor (VIN1-VIN3)can't connect to suspend power,change VIN1 to connect +12V
		15	1.ADD R504,R505 FOR codec GPI pull high or pull low 2.ADD C600 for SPDIFIN signal quility(option) 3.SIDESURR connect to J5C,SURR connect to J5A
		23	ADD R506,R507,Q70 FOR LATCH CIRCUIT
		26	ADD R500,R501 FOR CORRECT FAN sense value
		28	rename wrong net name(AVDD_5VA--->AVDD5, +12V_ASBY----->AVDD_12V)
	2005/01/25	27	D20,D21,D22 CONNECT TO V_2P5_MCH 1.FOR EMI: ADD C636 between GND&AGND
	2005/01/27	15	2.FOR EMI: ADD R508 at AC BITCLK FOR EMI:1.ADD C618-C629 connect to VCC_DDR,
	2005/01/27	18	2.ADD C630-C635 connect between VCC_DDR&VTT_DDR 3.ADD C611-C617 connect to VTT_DDR 4.ADD C601,C602 connect between VCC_DDR&VCC3
	2005/01/27	23	FOR EMI:1.ADD C603-C610 connect to +12V
0B	2005/03/14	8	FIX WRONG SWAP(H_BLO-H_BL2)
		15	R435 CHANGE TO 39.2K FOLLOW REALTEK SUGGESTED
		21	CS5 CHANGE TO 15P(MAKE THE SIGNAL RATTER)
		24	EC55 CHANGE TO 1000U/EC43 CHANGE TO 1800U(MAKE THE VOLTAGE STABLE)
		25	R212 CHANGE TO 1.69K/1K;R219 CHANGE TO 300K/1K(ADD EC20,EC33,EC32) FOR VCORE TRANSIEN ABOUT 2004 PERFORMANCE
		25	C270&C113 CHANGE TO 1U/16V/0805,PREVENT THE ENERGY OVER THE LIMITE OF RESISITOR
		26	ADD SYSTEM FAN DELAY CURCUITE

Rev	Date	Page	Description